Amendments to the Specification

Please replace paragraph **[0002]** with the following amended paragraph:

[0002] This application is related to U.S. Application No. 10/632,549, titled "Semiconductor multi-package module having wire bond interconnect between stacked packages"; U.S. Application No. 10/632,568, titled "Semiconductor multi-package module having package stacked over ball grid array package and having wire bond interconnect between stacked packages"; U.S. Application No. 10/632,551, titled "Semiconductor multi-package module having wire bond interconnect between stacked packages and having electrical shield", which issued on January 4, 2005 as U.S. Patent No. 6,838,761; U.S. Application No. 10/632,552, titled "Semiconductor multi-package module having package stacked over die-up flip chip ball grid array package and having wire bond interconnect between stacked packages"; U.S. Application No. 10/632,553, titled "Semiconductor multi-package module having package stacked over die-down flip chip ball grid array package and having wire bond interconnect between stacked packages"; U.S. Application No. 10/632,550, titled "Semiconductor multi-package module including stacked-die packages and having wire bond interconnect between stacked packages". This application and all the said related applications are being filed on the same date, and each of the said related applications is hereby incorporated herein by reference.

Please replace paragraph **[0068]** with the following amended paragraph:

[0068] In the top LGA package in the embodiment of FIG. **5A** the die is wire bonded onto wire bond sites on the upper metal layer of the substrate to establish electrical connections. The die **514** and the wire bonds **516** are encapsulated with a molding compound **517** that provides protection from ambient and from mechanical stress to facilitate handling operations, and has a top package upper surface **519**. The top package **500** is stacked over the bottom package **400** and affixed there using an adhesive [[**513**]] **503**. Solder masks **515, 527** are patterned over the metal layers **521, 523** to expose the underlying metal at bonding sites for electrical connection, for example the wire bond sites for bonding the wire bonds **516**..